

NCE N-Channel Enhancement Mode Power MOSFET

Description

The NCE82H140D uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

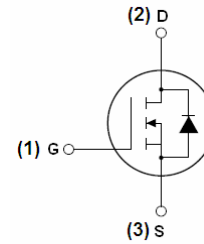
- $V_{DS} = 82V, I_D = 140A$
 $R_{DS(ON)} < 5.2m\Omega @ V_{GS}=10V$ (Typ:4.3m Ω)
- Special process technology for high ESD capability
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

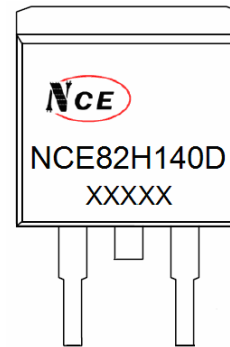
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

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100% ΔV_d s TESTED!



Schematic diagram



Marking and pin assignment



TO-263-2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE82H140D	NCE82H140D	TO-263-2L	-	-	-

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	82	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	140	A
Drain Current-Continuous($T_C=100^\circ C$)	$I_D(100^\circ C)$	99	A
Pulsed Drain Current ^(Note 1)	I_{DM}	480	A
Maximum Power Dissipation	P_D	220	W
Derating factor		1.47	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	1500	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta Jc}$	0.68	$^{\circ}C/W$
Thermal Resistance, Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	60	$^{\circ}C/W$

Electrical Characteristics ($T_C=25^{\circ}C$ unless otherwise noted)

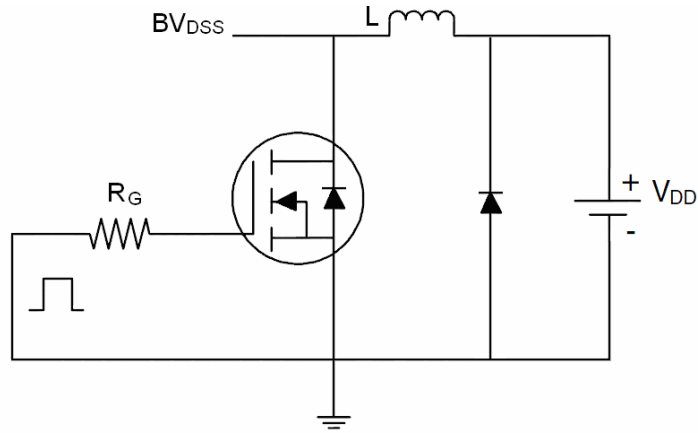
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	82	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=82V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.5	3	3.8	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=20A$	-	4.3	5.2	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=20A$	65	-	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=40V, V_{GS}=0V,$ $F=1.0MHz$	-	7900	-	PF
Output Capacitance	C_{oss}		-	445	-	PF
Reverse Transfer Capacitance	C_{rss}		-	384	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, R_L=1\Omega$ $V_{GS}=10V, R_{GEN}=2.5\Omega$	-	23	-	nS
Turn-on Rise Time	t_r		-	42	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	75	-	nS
Turn-Off Fall Time	t_f		-	26	-	nS
Total Gate Charge	Q_g	$V_{DS}=40V, I_D=20A,$ $V_{GS}=10V$	-	158	-	nC
Gate-Source Charge	Q_{gs}		-	32	-	nC
Gate-Drain Charge	Q_{gd}		-	51	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_S=140A$	-	-	1.2	V
Diode Forward Current ^(Note 2)	I_S	-	-	-	140	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}C, I_F = 20A$ $di/dt = 100A/\mu s$ ^(Note 3)	-	50	-	nS
Reverse Recovery Charge	Q_{rr}		-	110	-	nC

Notes:

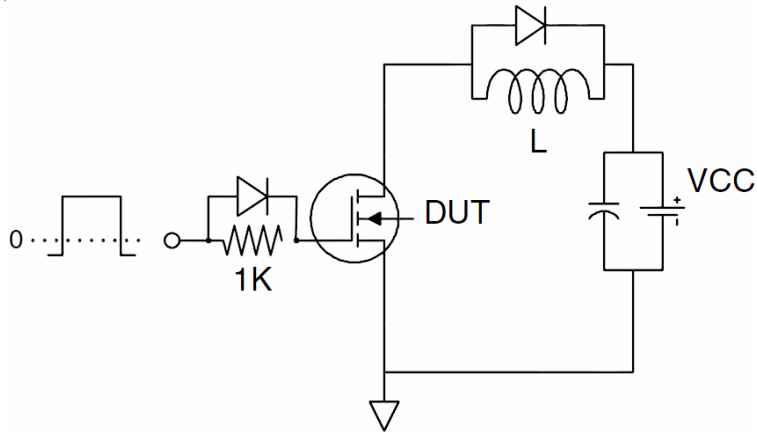
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}C, V_{DD}=40V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test circuit

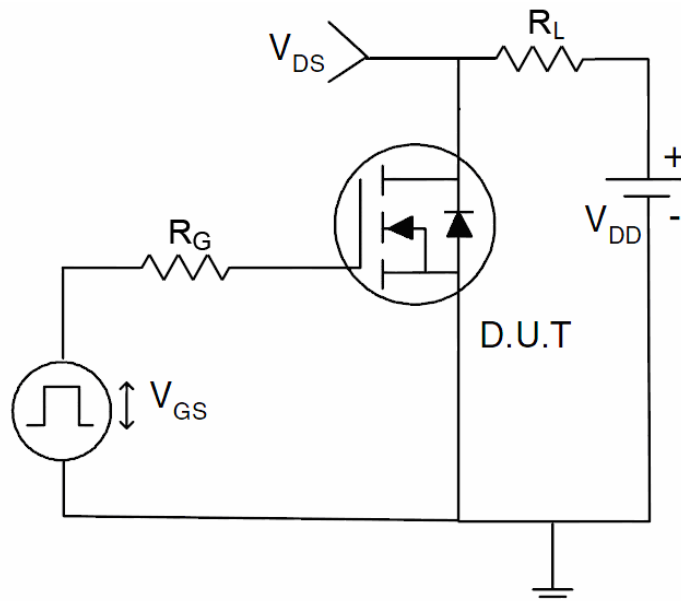
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

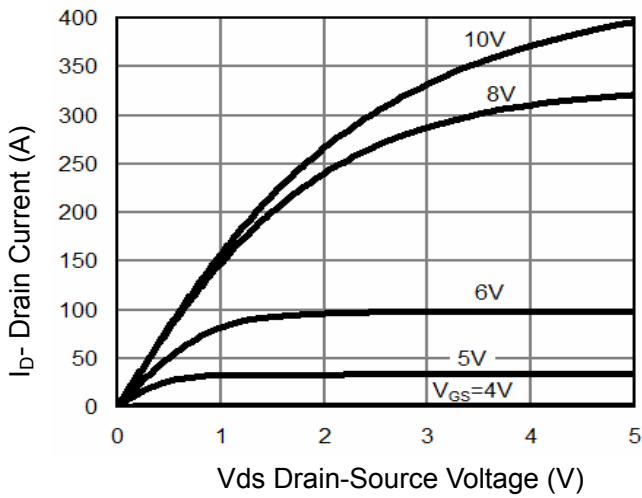


Figure 1 Output Characteristics

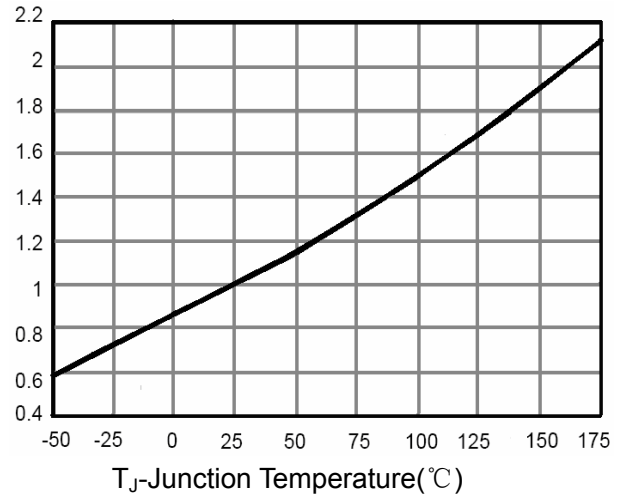


Figure 4 $R_{DS(on)}$ -Junction Temperature

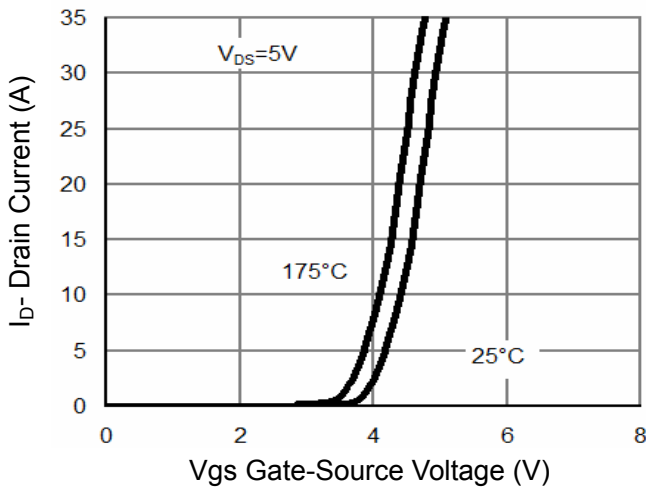


Figure 2 Transfer Characteristics

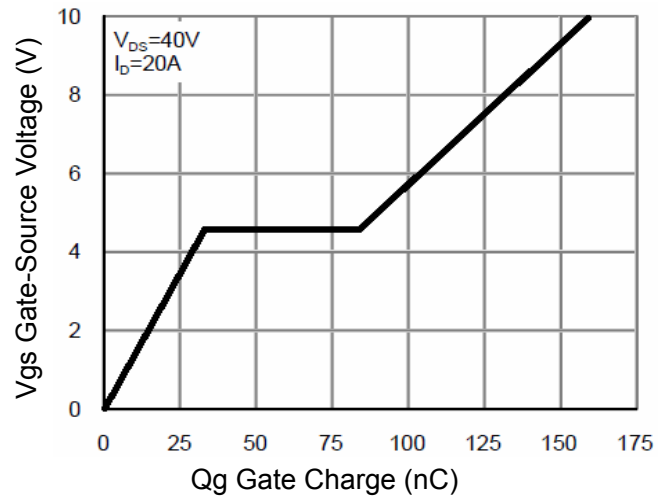


Figure 5 Gate Charge

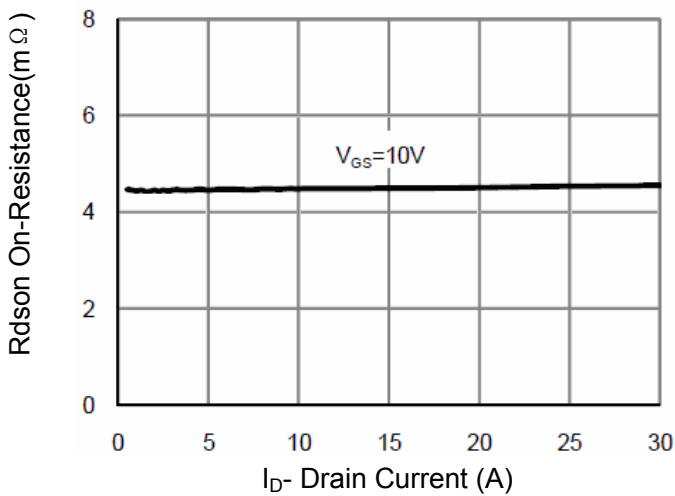


Figure 3 $R_{DS(on)}$ - Drain Current

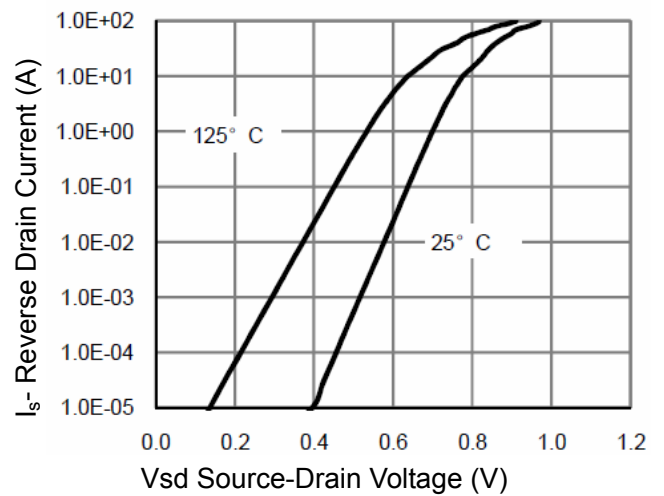


Figure 6 Source- Drain Diode Forward

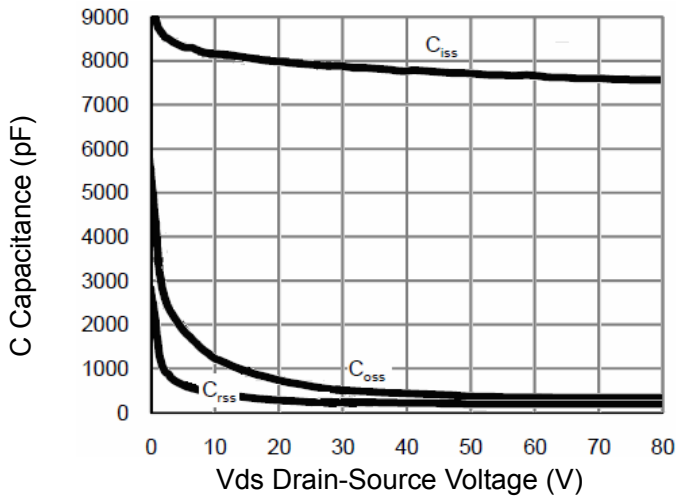


Figure 7 Capacitance vs Vds

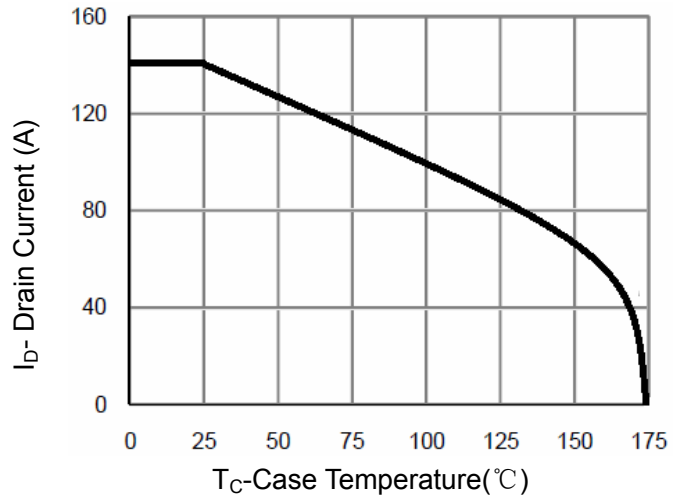


Figure 9 Current De-rating

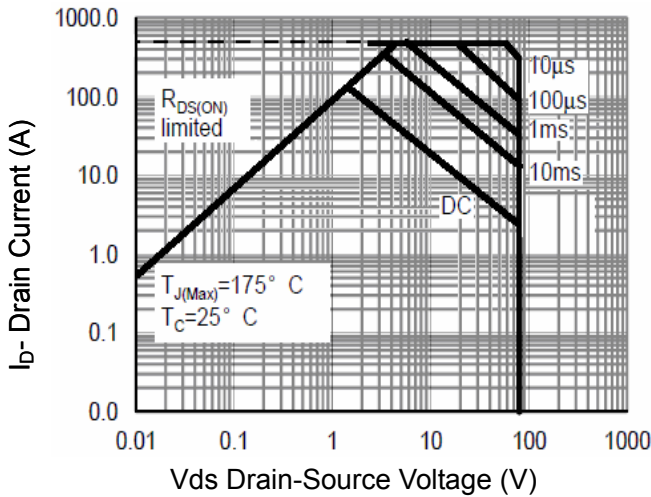


Figure 8 Safe Operation Area

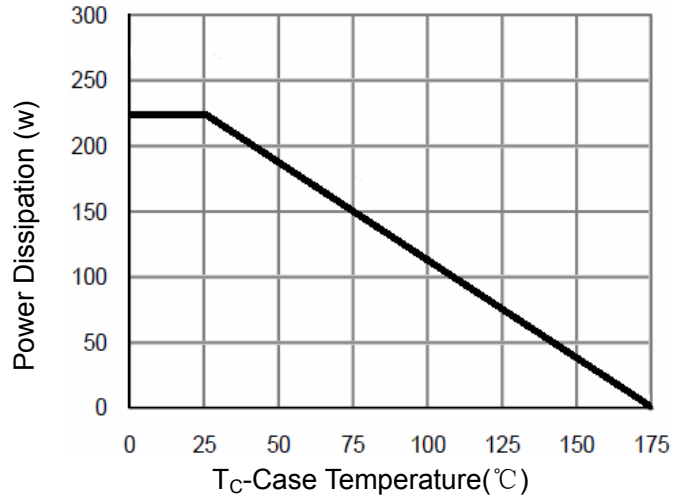


Figure 10 Power De-rating

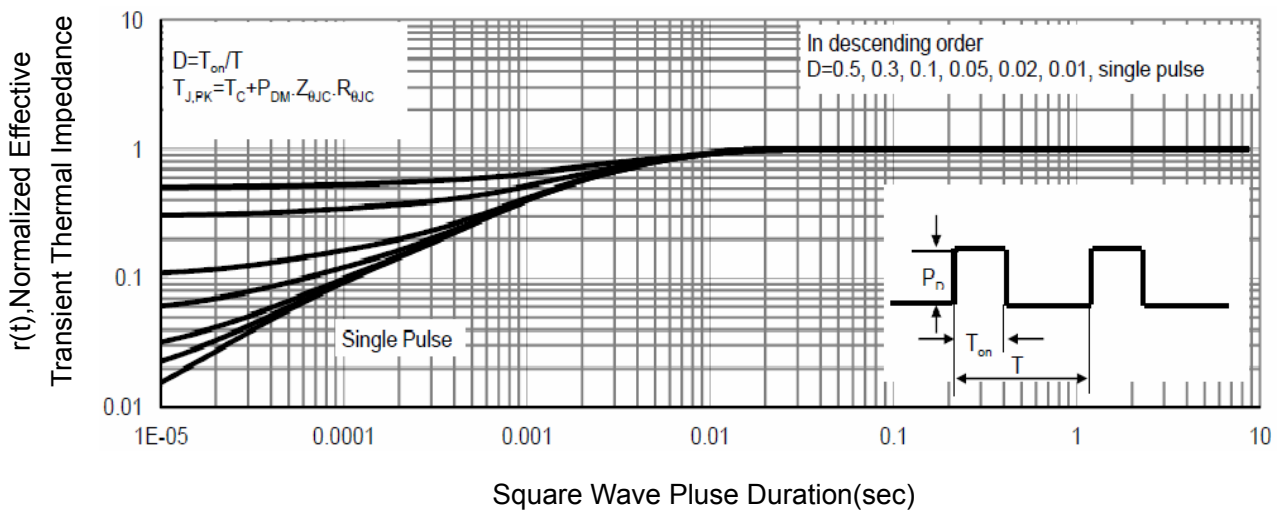
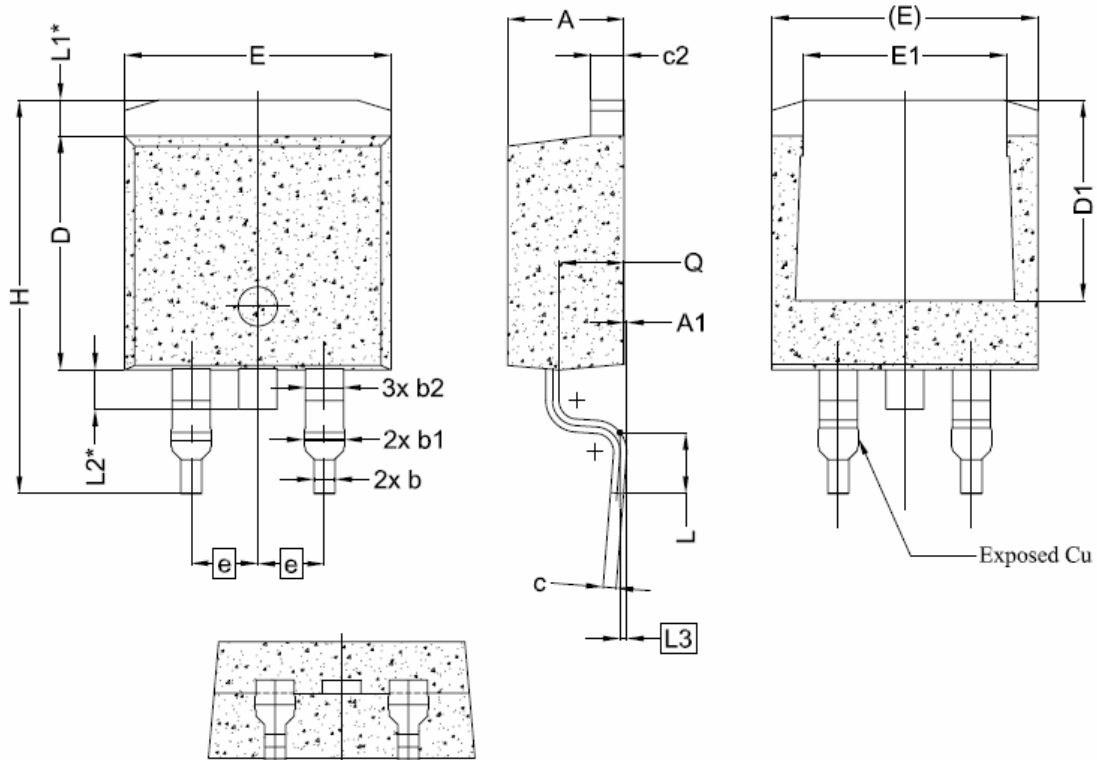
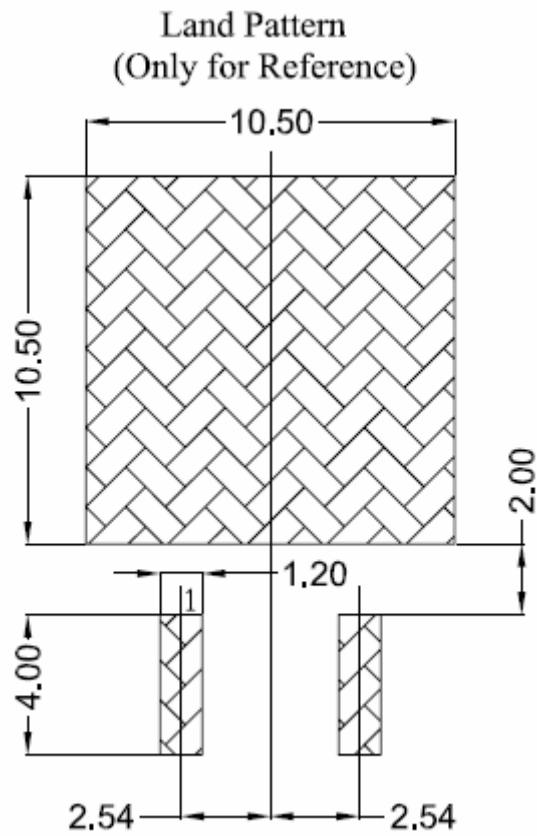


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-263-2L Package Information



Symbol	Dimensions In Millimeters		
	Min.	Nom.	Max.
A	4.24	4.44	4.64
A1	0.00	0.10	0.25
b	0.70	0.80	0.90
b1	1.20	1.55	1.75
b2	1.20	1.45	1.70
c	0.40	0.50	0.60
c2	1.15	1.27	1.40
D	8.82	8.92	9.02
D1	6.86	7.65	-
E	9.96	10.16	10.36
E1	6.89	7.77	7.89
e	2.54BSC		
H	14.61	15.00	15.88
L	1.78	2.32	2.79
L1	1.36 REF.		
L2	1.50 REF.		
L3	0.25 BSC		
Q	2.30	2.48	2.70



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